UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER OF PATENTS AND TRADEMARKS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/807,067	04/06/2001	Walter Jan August De Coster	PHQ99.010	2192

24737 7590 05/22/2003

PHILIPS ELECTRONICS NORTH AMERICAN CORP
580 WHITE PLAINS RD
TARRYTOWN, NY 10591

EXAMINER
GUERRERO, MARIA F

ART UNIT	PAPER NUMBER
2822	

DATE MAILED: 05/22/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/807,067	Applicant(s) DE COSTER ET AL.	
	Examiner Maria Guerrero	Art Unit 2822	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *06 March 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-9* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-9* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____.
4) ☐ Interview Summary (PTO-413) Paper No(s). _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

1. This Office Action is in response to the Amendment filed January 28, 2003 and the Request for continued examination filed March 6, 2003.

Claims 1-9 are pending.

Continued Examination Under 37 CFR 1.114

2. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on March 6, 2003 has been entered.

Priority

3. This Application is a 371 of PCT/EP00/07519 filed August 2, 2000.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4. Claim 6 is rejected under 35 U.S.C. 102(b) as being anticipated by Jiro Ida (JP 07-066406 (Translation).

Jiro Ida teaches an integrated circuit comprising lateral isolation regions formed at the sides of at least one projecting region of polysilicon (24) (Fig. 1c, paragraphs 0015-0016). Jiro Ida shows each lateral region being composed of a smaller isolation layer (26) and a larger isolation layer (28), each lateral isolation region comprising a vertical trench made in the smaller isolation layer (Fig. 1d-1e, paragraph 0017). Jiro Ida teaches the integrated circuit comprising a metal silicide (31, 49) situated in the upper part of the polysilicon region and having a planar surface that is higher than the larger isolation region (Fig. 1f, 3, paragraphs 0018-0024).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 1-5 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kawaguchi (U.S. 5,739,573) in view of Lur et al. (U.S. 6,013,569).

Kawaguchi teaches forming spacers at the sides of a projecting polysilicon region, the spacers having a smaller isolation layer in contact with the projecting polysilicon region, and a larger isolation layer (Fig. 5B-5B, col. 10, lines 10-33). Kawaguchi discloses anisotropically etching at least the vertical portion of the smaller isolation layer to form a trench, the trench being between the larger isolation layer and the corresponding side of the projecting polysilicon region, and the depth of trench

being equal to maximally half the height of the larger isolation layer and maximally half the thickness of the larger isolation layer (Fig. 5C, col. 10, lines 35-50). Kawaguchi teaches subjecting the projecting polysilicon region to a silicidation process by directional depositing a metal layer capable of forming a metal silicide (Fig. 5D-5E, col. 10, lines 65-67, col. 11, lines 1-30).

Kawaguchi teaches an integrated circuit comprising lateral isolation regions formed at the sides of at least one projecting region of polysilicon (Fig. 5B, 7B). Kawaguchi shows each lateral region being composed of a smaller isolation layer and a larger isolation layer, each lateral isolation region comprising a vertical trench made in the smaller isolation layer (Fig. 5C, 7C). Kawaguchi teaches the integrated circuit comprising a metal silicide situated in the upper part of the polysilicon region (Fig. 5E, 7E).

Kawachi does not specifically show the depth of the trench being measured from a top of the larger isolation layer down to the smaller isolation layer. However, Lur et al. teaches forming the spacers having a smaller isolation layer in contact with the projecting polysilicon region and a larger isolation layer (Fig. 7-8, col. 8, lines 10-35). Lur et al. discloses isotropically etching at least the vertical portion of the smaller isolation layer to form a trench, the trench being less than the half the height of the larger isolation layer from the top of the larger isolation layer down to the smaller isolation layer (Fig. 8, col. 8, lines 45-65). Lur et al. teaches subjecting the projecting polysilicon region to a silicidation process by directional depositing a metal layer capable of forming a metal silicide (Fig. 9, col. 9, lines 3-15, 35-45).

Therefore, It would have been obvious to a person of ordinary skill in the art at the time of the invention to modify Kawaguchi reference by including the teaching of Lur et al. in order to avoid stress to the sidewalls of the polysilicon line (Lur et al., Abstract).

6. Claims 7-9 are rejected under 35 U.S.C. 103(a) as being unpatentable over Jiro Ida (JP 07-066406) (Translation).

Regarding claims 7-9, Jiro Ida is silent about the depth of the trench. However, a person of ordinary skill in the art would recognize that the Jiro Ida's drawings implicitly disclosed the depth of the trench (Fig. 1).

Therefore, it would have been obvious to a person of ordinary skill in the art at the time of the invention to infer the depth of the trench being equal to maximally half the height of the larger isolation layer or at least $1/20^{th}$ of the height of the projecting region of the silicidized polysilicon in order to obtain low resistance.

Response to Arguments

7. Applicant's arguments with respect to claims 1-9 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

8. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Matsumoto et al. (U.S. 5,726,479) teaches forming a metal silicide layer including a planar surface and that is higher than the larger isolation layer. Ramaswami (U.S. 5,783,475) is cited to show that controlling the depth of the trench between the spacers is well known in the art.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Maria Guerrero whose telephone number is 703-305-0162.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Amir Zarabian can be reached on 703-308-49055. The fax phone numbers for the organization where this application or proceeding is assigned are 703-308-7722 for regular communications and 703-308-7724 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0956.

María Guerrero
Maria Guerrero
Patent Examiner
May 12, 2003